LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1.   (**Currently Amended**)   A semiconductor integrated circuit device having a dynamic RAM, said dynamic RAM comprising a memory array, a RAM control section, an ECC-codec circuit, and an ECC controller, said RAM control section comprising a command decoding section responsive to an external command from the outside of said dynamic RAM for decoding the external command and a super self-refresh control circuit, said super self-refresh control circuit being contained within said RAM control section, wherein:

said command decoding section is also adapted to receive an internal command generated inside said dynamic RAM and to decode the internal command;

said ECC controller comprising comprises a command generating section and an address generating section, said address generating section being contained within said ECC controller;

said command decoding section delivering delivers a start instruction signal representative of encoding to said ECC controller when an entry command is decoded as the external command;

said command generating section of said ECC controller delivering delivers, upon reception of the start instruction signal, a first operation mode signal representative of the encoding and simultaneously making makes said address generating section of said ECC controller sequentially generate addresses corresponding to operation timings of the first operation mode signal and supply supplies the addresses to said memory array;

said ECC-codec circuit carrying carries out, upon reception of the first operation mode signal, an encoding operation of producing a check bit for error detection/correction with reference to information data stored in said memory array and writing writes the check bit into a predetermined region of said memory array;

said command generating section of said ECC controller delivering delivers, upon completion of the encoding operation by said ECC-codec circuit, a first [[nd]] end signal as [[th]] the internal command to said command decoding section;

said super self-refresh control circuit of said RAM control section ~~starting~~ starts, when said command decoding section receives and decodes the first end signal as the internal command, a super self-refresh operation which has a refresh cycle lengthened within an allowable range of error occurrence by an error correcting operation using the check bit.

2.   (Original)   A semiconductor integrated circuit device as claimed in claim 1, wherein:

the entry command is supplied by a user to said dynamic RAM.

3.   (Currently Amended)   A semiconductor integrated circuit device as claimed in claim 1, wherein:

said command decoding section ~~delivering~~ delivers, when an exit command as the external command is decoded, a stop instruction signal representative of decoding to said ECC controller;

said super self-refresh control circuit of said RAM control section finishes the super self-refresh operation when said command decoding section decodes the exit command;

said command generating section of said ECC controller ~~delivering~~ delivers, upon reception of the stop instruction signal, a second operation mode signal representative of the decoding and simultaneously ~~making~~ makes said address generating section of said ECC controller sequentially generate addresses corresponding to operation timings of the second operation mode signal and ~~supply~~ supplies the addresses to said memory array;

said ECC-codec circuit ~~carrying~~ carries out, upon reception of the second operation mode signal, a decoding operation of reading the check bit for error detection/correction from the predetermined region of said memory array and ~~correcting~~ corrects, with reference to the check bit and the information data stored in said memory array, an [[rror]] error in [[th]] the information data to rewrite [[th]] the information data;

said command generating section of said ECC controller ~~delivering~~ delivers, upon completion of the ~~encoding~~ decoding operation by said ECC-codec circuit, a second end signal as the internal command to said command decoding section.

4.   (Currently Amended)   A semiconductor integrated circuit device as claimed in claim 3, wherein:

~~said command generator of said ECC controller delivers the second end signal to said command decoder of said RAM control section as the internal command upon completion of the decoding operation by said ECC-CODEC circuit;~~

said RAM control section automatically ~~starting~~ starts a self-refresh operation and ~~holding~~ holds data in response to the second end signal.

5.   (Currently Amended)   A semiconductor integrated circuit device as claimed in claim 3, wherein:

~~said command generator of said ECC controller delivers the second end signal to said command decoder of said RAM control section as the internal command upon completion of the decoding operation by said ECC-CODEC circuit;~~

said RAM control section subsequently ~~receiving~~ receives a refresh operation instruction from the outside and ~~holding~~ holds data.

6.   (Original)   A semiconductor integrated circuit device as claimed in claim 3, wherein:

the entry command and the exit command are supplied by a user to said dynamic RAM.

7.   (Currently Amended)   A semiconductor integrated circuit device having a dynamic RAM, said dynamic RAM comprising a memory array, a RAM control section, an error correction circuit, and a BIST (built-in self-test) controller, said RAM control section comprising a command decoding section responsive to an external command from the outside of said dynamic RAM for decoding the external command, wherein:

said command decoding section is also adapted to receive an internal command generated inside said dynamic RAM and to decode the internal command;

said BIST controller ~~comprising~~ comprises a command generating section and an address generating section, said address generating section being contained within said BIST controller;

said command decoding section ~~delivering~~ <u>delivers</u> a start instruction signal representative of checking to said ~~error correction circuit~~ <u>BIST controller</u> when a BIST entry command is decoded as the external command;

said command generating section of said BIST controller ~~delivering~~ <u>delivers</u>, upon reception of the start instruction signal, an operation mode signal representative of the checking and simultaneously ~~making~~ <u>makes</u> said address generating section of said BIST controller sequentially generate addresses corresponding to operation timings of the operation mode signal and ~~supply~~ <u>supplies</u> the addresses to said memory array;

said error correction circuit ~~producing~~ <u>produces</u>, upon reception of the operation mode signal, write data corresponding to the addresses sequentially generated, ~~writing~~ <u>writes</u> the write data into a predetermined region or an entire region of said memory array, ~~producing~~ <u>produces</u> expectation data corresponding to the addresses sequentially generated, ~~comparing~~ <u>compares</u> the expectation data with information data read from said memory array, ~~detecting~~ <u>detects</u> an error in the information data, and, upon completion of error detection, ~~delivering~~ <u>delivers</u> an end signal as the internal command to said command decoding section;

delivery of the ~~operation mode~~ <u>start instruction</u> signal being stopped when said command decoding section receives and decodes the end signal as the internal command.

8. (Original) A semiconductor integrated circuit device as claimed in claim 7, wherein:

the BIST entry command is supplied by a user to said dynamic RAM.

9. (Currently Amended) A semiconductor integrated circuit as claimed in claim 7, wherein:

said BIST controller further ~~compris s~~ <u>comprises</u> a register circuit which holds the result of the error detection;

said BIST controller ~~making~~ <u>makes</u> said register circuit deliver the result of error detection to the outside when said command decoder receives a readout instruction as the external command.

10. (Currently Amended)   A semiconductor integrated circuit device as claimed in claim 3, wherein:

said ECC-codec circuit further comprises a register circuit which holds an error detection signal of said ECC-codec circuit as a result of error detection;

said ECC-codec circuit ~~making~~ <u>makes</u> said register circuit deliver the result of error detection to the outside when said command decoder receives a readout instruction as the external command.

11. (Currently Amended)   A semiconductor integrated circuit device as claimed in claim 3, wherein:

said ECC controller further comprises a register circuit which holds an error location detection instruction of said ECC controller as a result of the error detection;

said ECC controller ~~making~~ <u>makes</u> said register circuit deliver the result of error detection to the outside when said command decoder receives a readout instruction as the external command.

12. (Original)   A semiconductor integrated circuit device as claimed in claim 3, wherein:

sequential decoding is used in decoding an error correction code in said super self-refresh operation, error location detection being executed by backward cyclic shift of a cyclic shift register, other operations being executed by forward cyclic shift.